

Very Low Noise, High Accuracy, Quad Universal Filter Building Block

February 1998

FEATURES

- **Four Identical 2nd Order Filters in an SSOP Package**
- **Clock-to-Center Frequency Ratio: 200:1**
Internal Sampling Rate to Center Frequency Ratio: 400:1
- **Center Frequency Error: $\pm 0.3\%$ (Typ)**
- **Low Noise: $\leq 40\mu V_{RMS}$ per 2nd Order Section, $Q \leq 5$**
- **High Dynamic Range: $THD + Noise \leq 0.01\%$**
- **Low DC Offsets: $\leq 10mV$ per 2nd Order Section**
- **No Aliasing for Input Frequencies up to $400 \times f_{CUTOFF}$**
- **Center Frequency up to 25kHz ($V_S = \pm 5V$)**
- **Operates from $\pm 1.57V$ to $\pm 5V$ Power Supplies**

APPLICATIONS

- Over Sampled Lowpass Filters, $f_c \leq 25kHz$
- Precision Highpass Filters
- Notch Filters with 60dB or More Notch Depth
- Audio Equalizer Filters
- Noise Cancellation Filters

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DESCRIPTION

The LTC[®]1068-200 consists of four identical, low noise, high accuracy 2nd order switched-capacitor filter building blocks. Each building block, together with three to five resistors, can provide 2nd order filter functions like low-pass, bandpass, highpass and notch. High precision, high performance, quad 2nd order, dual 4th order or 8th order filters can be designed with an LTC1068-200. The center frequency of each 2nd order section is tuned by an external clock. The clock-to-center frequency ratio is internally set to 200:1 and can be modified by external resistors.

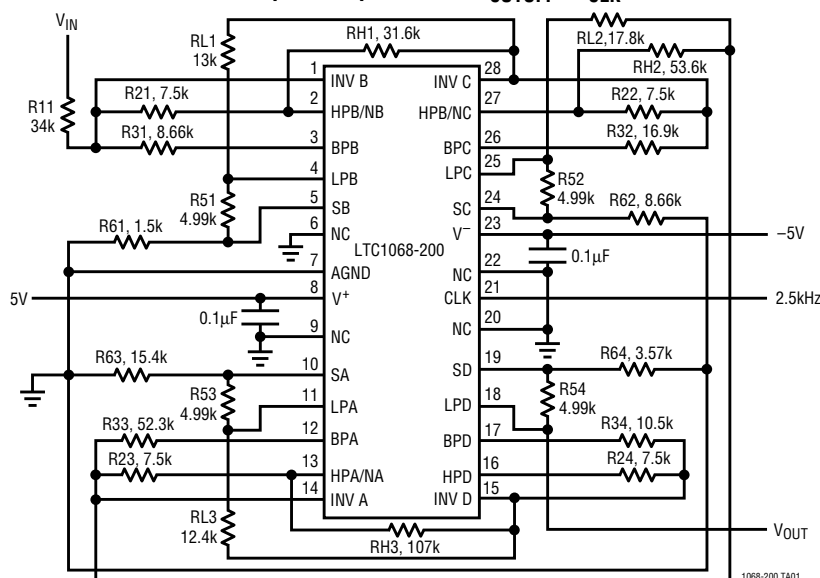
The sampling rate of the LTC1068-200 is twice the clock frequency. The maximum input frequency can approach twice the clock frequency before aliasing occurs.

A customized version of the LTC1068-200 in a 16-lead SO with internal thin film resistors can be obtained. Clock-to-center frequency ratios higher or lower than 200:1 can also be obtained. Please contact LTC Marketing for details.

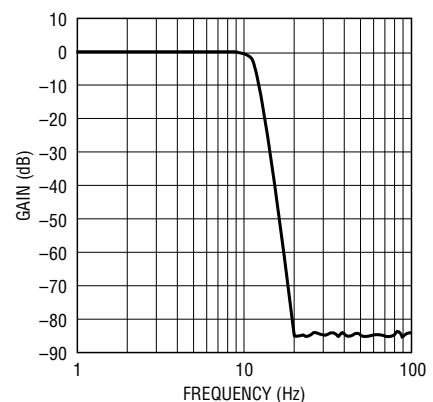
The LTC1068-200 is available in a 28-pin SSOP surface mount package and is supported by FilterCAD[™] 2.0 filter design software.

TYPICAL APPLICATION

10Hz, Elliptic Lowpass Filter, $f_{CUTOFF} = f_{CLK}/250$



Frequency Response



1068-200 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	12V
Power Dissipation	500mW
Operating Temperature Range	
LTC1068CG-200	0°C to 70°C
LTC1068IG-200	-40°C to 85°C
Input Voltage at Any Pin ... $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$	
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
INV B [1]	[28] INV C	LTC1068CG-200 LTC1068IG-200
HPB/NB [2]	[27] HPC/NC	
BPB [3]	[26] BPC	
LPB [4]	[25] LPC	
SB [5]	[24] SC	
NC [6]	[23] V^-	
AGND [7]	[22] NC	
V^+ [8]	[21] CLK	
NC [9]	[20] NC	
SA [10]	[19] SD	
LPA [11]	[18] LPD	
BPA [12]	[17] BPD	
HPA/NA [13]	[16] HPD/ND	
INV A [14]	[15] INV D	
G PACKAGE 28-LEAD PLASTIC SSOP $T_{JMAX} = 125^\circ\text{C}$, $\theta_{JA} = 95^\circ\text{C/W}$		

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $V_S = \pm 5V$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		± 1.57		± 5.5	V
Voltage Swings	$V_S = 3.14V$, $R_L = 5k$ (Note 1)	●	1.2	1.6	V_{P-P}
	$V_S = 4.75V$, $R_L = 5k$ (Note 1)	●	2.6	3.2	V_{P-P}
	$V_S = \pm 5V$, $R_L = 5k$	●	± 3.4	± 4.1	V
Output Short-Circuit Current (Source/Sink)	$V_S \leq 4.75V$		17/6		mA
	$V_S = \pm 5V$		20/15		mA
DC Open-Loop Gain	$R_L = 5k$		85		dB
GBW Product			6		MHz
Slew Rate			10		V/ μs

(Complete Filter) $V_S = \pm 5V$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock-to-Center Frequency, f_{CLK}/f_0 (Note 5)	$V_S = 4.75V$, $f_{CLK} = 1\text{MHz}$, Mode 1 (Note 2), $f_0 = 5\text{kHz}$, $Q = 5$, $V_{IN} = 0.5V_{RMS}$, $R1 = R3 = 49.9k$, $R2 = 10k$	●	$200 \pm 0.3\%$	$200 \pm 0.8\%$ $200 \pm 0.9\%$	
	$V_S = \pm 5V$, $f_{CLK} = 1\text{MHz}$, Mode 1, $f_0 = 5\text{kHz}$, $Q = 5$, $V_{IN} = 1V_{RMS}$, $R1 = R3 = 49.9k$, $R2 = 10k$	●	$200 \pm 0.3\%$	$200 \pm 0.8\%$ $200 \pm 0.9\%$	
Clock-to-Center Frequency Ratio, Side-to-Side Matching (Note 5)	$V_S = 4.75V$, $f_{CLK} = 1\text{MHz}$, $Q = 5$ (Note 2)	●	± 0.25	± 0.9	%
	$V_S = \pm 5V$, $f_{CLK} = 1\text{MHz}$, $Q = 5$	●	± 0.25	± 0.9	%
Q Accuracy (Note 5)	$V_S = 4.75V$, $f_{CLK} = 1\text{MHz}$, $Q = 5$ (Note 2)	●	± 1	± 3	%
	$V_S = \pm 5V$, $f_{CLK} = 1\text{MHz}$, $Q = 5$	●	± 1	± 3	%

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 5V$, $T_A = 25^\circ C$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
f_0 Temperature Coefficient			± 1		ppm/ $^\circ C$
Q Temperature Coefficient			± 5		ppm/ $^\circ C$
DC Offset Voltage (Note 5) (See Table 1)	$V_S = \pm 5V$, $f_{CLK} = 1MHz$, V_{OS1} (DC Offset of Input Inverter)	●	0	± 15	mV
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$, V_{OS2} (DC Offset of First Integrator)	●	± 2	± 25	mV
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$, V_{OS3} (DC Offset of Second Integrator)	●	± 5	± 40	mV
Clock Feedthrough	$V_S = \pm 5V$, $f_{CLK} = 1MHz$		0.1		mV _{RMS}
Maximum Clock Frequency (Note 4)	$V_S = \pm 5V$, $Q \leq 2.0$, Mode 1		5.6		MHz
Power Supply Current	$V_S = 3.14V$, $f_{CLK} = 1MHz$ (Note 1)	●	3.5	8	mA
	$V_S = 4.75V$, $f_{CLK} = 1MHz$ (Note 2)	●	6.5	11	mA
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$	●	9.5	15	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Production testing for single 3.14V supply is achieved by using the equivalent dual supplies of $\pm 1.57V$.

Note 2: Production testing for single 4.75V supply is achieved by using the equivalent dual supplies of $\pm 2.375V$.

Note 3: Pin 7 (AGND) is the internal analog ground of the device. For single supply applications this pin should be bypassed with a $1\mu F$ capacitor. The biasing voltage of AGND is set with an internal resistive divider from Pin 8 to Pin 23 (see Block Diagram).

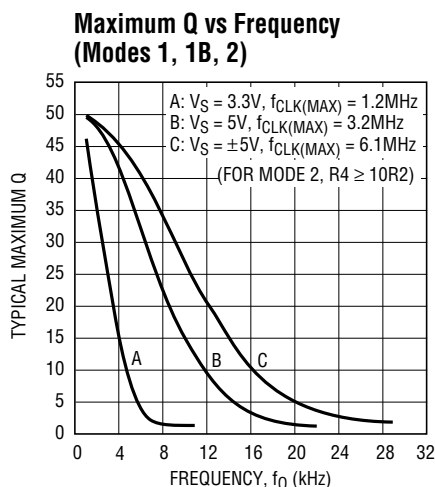
Note 4: See typical performance characteristics.

Note 5: Side D is guaranteed by design.

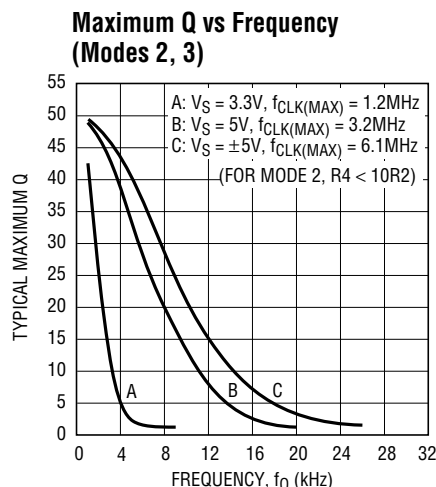
Table 1. Output DC Offsets One 2nd Order Section

MODE	V_{OSN}	V_{OSBP}	V_{OSLP}
1	$V_{OS1}[(1/Q) + 1 + H_{OLP}] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1B	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\sim (V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)X$ $[R4/(R2 + R4)] + V_{OS2}(R2/(R2 + R4))]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}[1 + R4/R1 + R4/R2 + R4/R3] - V_{OS2}(R4/R2) - V_{OS3}(R4/R3)$

TYPICAL PERFORMANCE CHARACTERISTICS

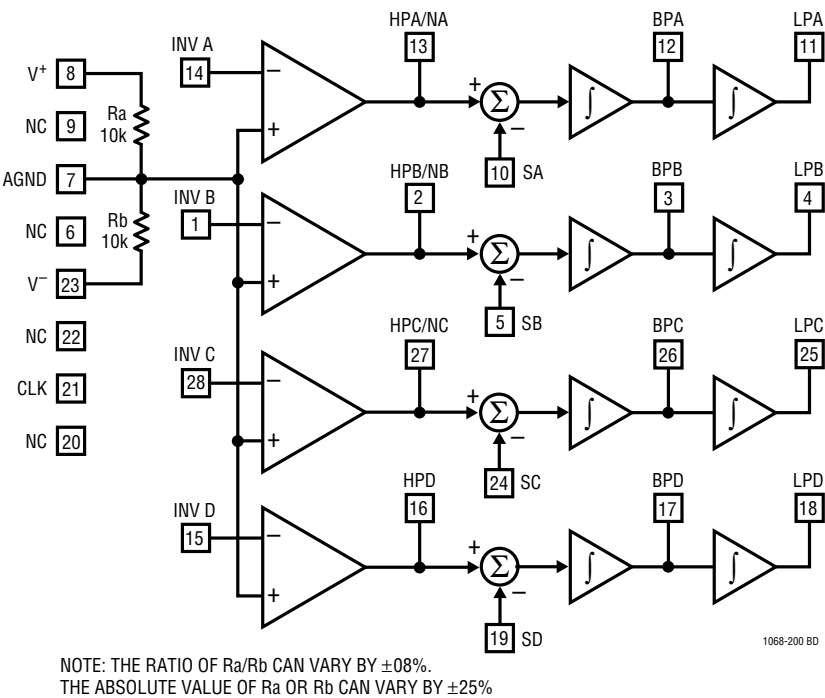


1068-200 G01



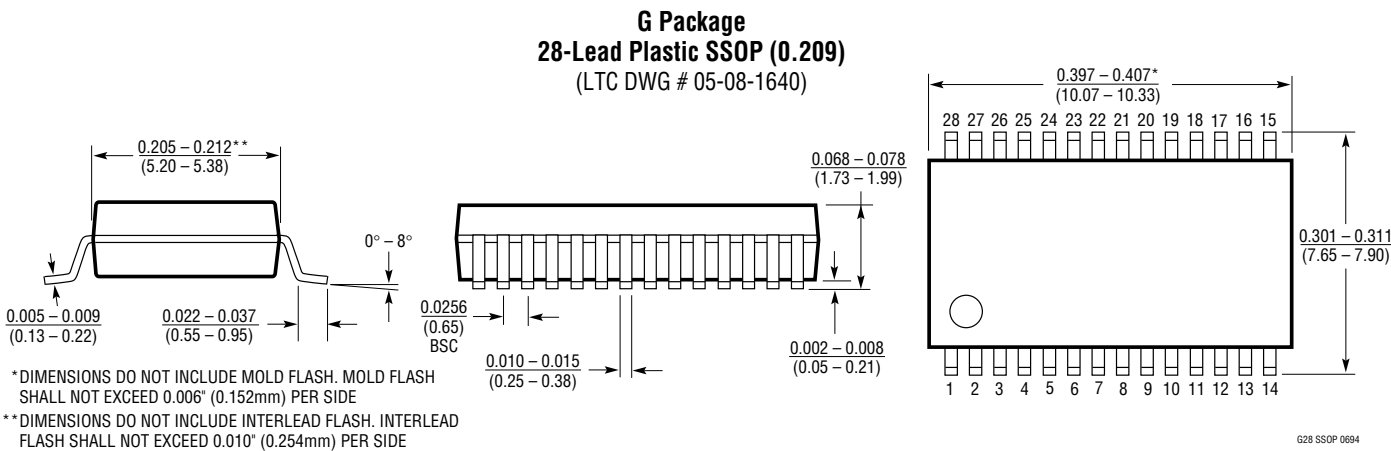
1068-200 G02

BLOCK DIAGRAM



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1068	Low Noise Universal Filter	100:1 Clock-to- f_0 Ratio, f_c to 50kHz
LTC1068-25	High Speed Universal Filter	25:1 Clock-to- f_0 Ratio, f_c to 200kHz
LTC1068-50	Low Power Universal Filter	50:1 Clock-to- f_0 Ratio, f_c to 25kHz
LTC1064	Universal Filter	50:1 and 100:1 Clock-to- f_0 Ratios, f_c to 100kHz, V_S = Up to $\pm 7.5V$
LTC1164	Low Power Universal Filter	50:1 and 100:1 Clock-to- f_0 Ratios, f_c to 20kHz, V_S = Up to $\pm 7.5V$
LTC1264	High Speed Universal Filter	20:1 Clock-to- f_0 Ratio, f_c to 200kHz, V_S = Up to $\pm 7.5V$